User Manual
FnIO S-Series
Special Function Module

List of Revisions

No.	Date	Version	Revision
1	2007.12.15	1.00	created

Contents

1. Product Specifications

1) Environment Specifications

Item		Specifications	Remarks
Temperature	Operating	0℃ to +60℃ (32°F to 140°F)	5101, 5111
		-20℃ to 55℃ (-4°F to 131°F)	
	Storage	-40℃ to +85℃ (-40°F to 185°F)	
Humidity	Operating	5 to 95% RH (Non-condensing)	
	Storage	5 to 95% RH (Non-condensing)	
Operating Altitude		2,000m	
Mounting		DIN Rail	

2) General Specifications

Item		Specifications	Remarks
Wiring I/O Cable		Max. 2.0m², AWG 14	
Shock Operating		10G	
Shock Non-Operating		30G	
Vibration/Shock Resistance	Displacement	0.012 Inch p-p from 10~57Hz	
	Acceleration	2G's from 57~500Hz	
	Sweep Rate	1 octave per Minute	
	Axes to test	X, Y, Z	
	Frequency Sweep per Axis	10	
EMC		Confirms to EN-61000-6-2	
EMI		Confirms to EN-61000-6-4	
Installation Pos. / Protect. Class		Variable / IP20	
Certifications		UL, cUL, CE	

2. High Speed Counter Module

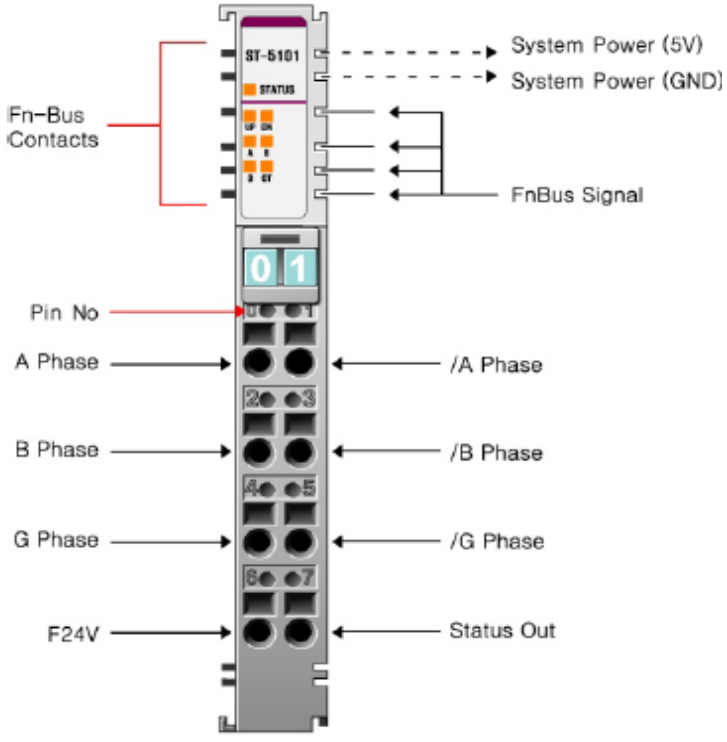
Description

- ST-51xx series is 1Channel encoder input module.
- It can count Binary pulse.
- It has all 7 LED for status indication.
  One is for FnBus, the others are for Input/Output status of Module.
- The 1Channel output for status indication is also provided together.
- It is isolated between Field I/O and FnBus by using Photo-coupler.
- It is operated regardless of Field Power supply. When the supplied Field Power has changed, the Expansion Field Power Supply (ST-7241) is required to be used absolutely.

1) ST-5101

- 1 channel Incremental Encoder Interface Terminal Type

◆ **Module View**



Mapping Data into the image table

◆ **I/O Process Image Table**

- Input Data

Byte Offset	Decimal Bit							
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Byte #0	Current Count Value (Low) when IDS=0 Stored Count Value (Low) when IDS=1							
Byte #1	Current Count Value (Low) when IDS=0 Stored Count Value (Low) when IDS=1							
Byte #2	Current Count Value (Low) when IDS=0 Stored Count Value (Low) when IDS=1							
Byte #3	Always 0							
Byte #4	Status Low (Compared flags)							
	0	0	SUF	SOF	SEQL	SEQ	SLT(<)	SGT(>)
Byte #5	Status High (same as LED Display)							
	0	0	SOT	SGIN	SBIN	SAIN	SDN	SUP

- Output Data

Byte Offset	Decimal Bit							
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Byte #0	Output Terminal (OT) Control							
	Output Terminal Selection "0000" : Force Off "0001" : GT "0010" : LT "0011" : EQ "0101" : Overflow "0110" : Underflow "1001" : CountUp "1010" : CountDown "1011" : A Terminal Input "1100" : B Terminal Input "1101" : G Terminal Input "1110" : PWM Output "1111" : Force On Others : Force Off				Output Terminal Pulse Width "0000" : Bypass "0001" : 1msec "0010" : 5msec "0011" : 10msec "0100" : 20msec "0101" : 50msec "0110" : 100msec "0111" : 200msec "1000" : 500msec "1111" : Latched Others : Bypass			
Byte #1	Command or PWM duty value (PWM Output Mode)							
	Command	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		HRST	CR	CP	CST	PU	PO	PE	IDS
	PWM Duty value	0~100dec (=0~100%)							

◆ **Input Data Byte #4**

SUF : Status Underflow (Latched)

SOF : Status Overflow (Latched)
SEQL(=) : Status Current count value = Compare count value (Latched)
SEQ(=) : Status Current count value = Compare count value (Unlatched)
SLT(<) : Status Current count value < Compare count value (Unlatched)
SGT(>) : Status Current count value > Compare count value (Unlatched)

◆ **Input Data Byte #5**

SOT : Status Output Terminal (same as OT)
SGIN : Status G Terminal Input
SBIN : Status B Terminal Input
SAIN : Status A Terminal Input
SDN : Status Counter Down
SUP : Status Counter Up

◆ **Output Data Byte #1**

HRST : HSC Reset
CR : Counter Reset, Current count value=0
CP : Counter Preset, Current count value=Initial count value
CST : Clear Status (SOT,SUF,SOF,SEQL)
PO : Process Overflow
PU : Process Underflow
PE : Process Equal
IDS : Input Data Selection(0:Current count value, 1:Store count value)

◆ **Specification**

Input Specification

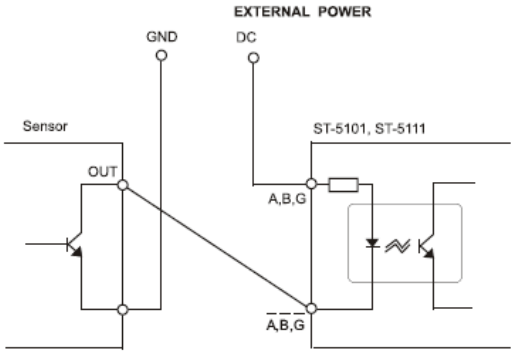
Input Voltage	5Vdc
Input Current	16.2mA@5Vdc
Input On-State Current	Input Current≥5mA
Input On-State Voltage	Input Voltage≥2.6Vdc
Output On-State Current	Input Current≤0.25mA
Output On-State Voltage	Input Voltage≤1.25Vdc
Max. On-State Voltage	6V
Max. Input Frequency	Max. 1.5MHz
Input filter selections	Bypass, 1㎲, 5㎲, 10㎲, 50㎲, 100㎲, 500㎲, 1㎳, 5㎳, 10㎳
Number of Inputs	0-1 group of A and /A(or GND) 2-3 group of B and /B(or GND) 4-5 group of G and /G(or GND)
Output Specification	
Number Of Output	6-7 States Output
Output Control	Output and be tied to any of 13State
Output Supply Voltage Range	5 to 28.8Vdc (HSC Status Output)
On State Current	Max. 1mA
Output Signal Delay	OFF to ON : Max. 0.5ms ON to OFF : Max. 1ms
Output Current Rating	Max. 0.5A
Output Type	Sink Type
Over Current Protection	1.8A(Shutdown Current)
Module Specification	
Power Dissipation	Max. 80mA @ 5.0Vdc
Isolation	I/O to Logic : Photo-coupler Isolation
	Field Power : Not Connected
Weight	70g
Size	12mm × 99mm × 70mm

◆ **Wiring Description**

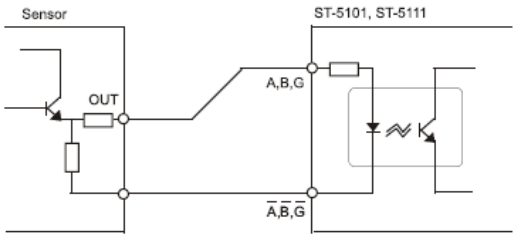
Pin No.	Description	Pin No.	Description
0	A Pulse Input	1	/A Pulse Input
2	B Pulse Input	3	/B Pulse Input
4	G Pulse Input	5	/G Pulse Input
6	F24V	7	Status Output(Sink)

CREVIS

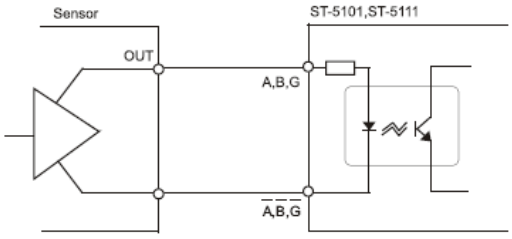
(1) Open Collector



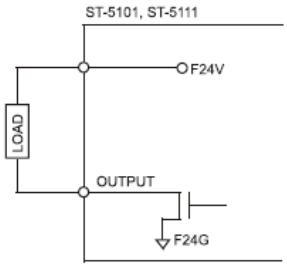
(2) VOLTAGE OUTPUT



(3) LINE DRIVE



(4) SINK OUTPUT (STATUS)



◆ **Configuration Parameter Table**

Offset	Access						Description
Byte#0	R/W	00-03	3	2	1	0	Counter Mode
			0	0	0	0	Counter Disabled
			0	0	0	1	1Pulse Mode (A:Pulse,B:Direction)
			0	0	1	0	2Pulse Mode (A:UpPulse,B:DownPulse)
			0	0	1	1	Encoder x1 (A:Aph B:Bph)
			0	1	0	0	Encoder x2 (A:Aph B:Bph)
			0	1	0	1	Encoder x4 (A:Aph B:Bph)
			0	1	1	0	Period/Rate Mode (Gate Function Disabled)
			0	1	1	1	Reserved
			1	0	0	0	PWM Output Mode (Gate Function Disabled)
			1	0	0	1	Reserved
			Others				Counter Disabled
		04-07	7	6	5	4	Gate Function
			0	0	0	0	Gate Function Disable
			0	0	0	1	Store/Continue
			0	0	1	0	Store/Wait/Resume
			0	0	1	1	Store-Reset/Wait/Start
			0	1	0	0	Store-Reset/Start
			Others				Gate Function Disabled
Byte#1		00-03	3	2	1	0	Input Filter
			0	0	0	0	Bypass (about 1.5㎒)
			0	0	0	1	1㎲±40%
			0	0	1	0	5㎲±40%
			0	0	1	1	10㎲±40%
			0	1	0	0	50㎲±40%
			0	1	0	1	100㎲±40%
			0	1	1	0	500㎲±40%
			0	1	1	1	1㎳±40%
			1	0	0	0	5㎳±40%
			1	0	0	1	10㎳±40%
			Others				Bypass (about 1.5㎒)
		04-07	7	6	5	4	Gate Sampling Time
			0	0	0	0	(10/1)㎒ (0.1㎲)
			0	0	0	1	(10/2)㎒ (0.2㎲)
			0	0	1	0	(10/4)㎒ (0.4㎲)
			0	0	1	1	(10/8)㎒ (0.8㎲)
			0	1	0	0	(10/16)㎒ (1.6㎲)
			0	1	0	1	(10/32)㎒ (3.2㎲)
			0	1	1	0	(10/64)㎒ (6.41㎲)
			0	1	1	1	(10/128)㎒ (12.8㎲)
			Others				(10/1)㎒ (0.1㎲)

◆ Memory Register Map

Byte Offset	Access	Description	Default Value
0	R	Current count value (Low byte) **(Input Data Byte #0)**	0x00
1	R	Current count value (Middle byte) **(Input Data Byte #1)**	0x00
2	R	Current count value (High byte) **(Input Data Byte #2)**	0x00
3	R	Always 0 **(Input Data Byte #3)**	0x00
4	R	Status Low (compared flags) **(Input Data Byte #4)**	0x00
5	R	Status High (same as LED display) **(Input Data Byte #5)**	0x00
6	R	Output Terminal (OT) Control **(Output Data Byte #0)**	0x00
7	R	SSR (Special Selection Register) **(Output Data Byte #1)**	0x00
8	R/W	Gate Function/Counter Mode **(Parameter Byte #0)**	0x00
9	R/W	Gate Sampling Time/Input Filter **(Parameter Byte #1)**	0x00
10	R/W	Don't care	0x00
11	R/W	Don't care	0x00
12	R	Stored count value (Low byte) **(Input Data Byte #0)**	0x00
13	R	Stored count value (Middle byte) **(Input Data Byte #1)**	0x00
14	R	Stored count value (High byte) **(Input Data Byte #2)**	0x00
15	R	Always 0 **(Input Data Byte #3)**	0x00
16	R/W	Initial Counter Value (Low Byte) (Initial counter or PWM Frequency value)	0x00
17	R/W	Initial Counter Value (Middle Byte) (Initial counter or PWM Frequency value)	0x00
18	R/W	Initial Counter Value (High Byte) (Initial counter or PWM Frequency value)	0x00
19	R/W	Always 0	0x00
20	R/W	Compare count value (Low byte)	0x00
21	R/W	Compare count value (Middle byte)	0x00
22	R/W	Compare count value (High byte)	0x00
23	R/W	Always 0	0x00

PWM Frequency = 1~20000(=1Hz~20KHz). If <0 then Off, if>20000 then 20KHz. (see Setting PWM Frequency value)
PWM Duty = 0 ~ 100 (= 0 ~ 100%). If >100 then 100% (see When used PWM duty value) (see When used PWM duty value)
PWM Output Mode uses Current counter to generate a continuous rolling down count sequence of numbers.
In Order to use normal PWM Output Mode, Output Terminal Selection=PWM Output, Output Terminal Pulse Width= Bypass. (see Status Output Terminal Control)
* See Register Description for the definition of the registers

◆ Register Description

Current counter value

- This Current counter value is really counting value of incoming pulse.
- This Current counter value can only reading to binary number (0 to 16,777,215).

Status Low (compared flags)

- This Status Low can only read.
- Operate of Status Low shows table with description.

Bit	7	6	5	4	3	2	1	0
Status Low	0	0	SUF	SOF	SEQL	SEQ	SLT	SGT

- SGT : Status Current counter value > Compare counter value (Unlatched)
- SLT : Status Current counter value < Compare counter value (Unlatched)
- SEQ : Status Current counter value = Compare counter value (Unlatched)
- SEQL : Status Current counter value = Compare counter value (Latched)
- SOF : Status Overflow (Latched)
- SUF : Status Underflow (Latched)

Status High (same as LED display)

- This Status High can only read.
- Operate of Status Low shows table with description.

Bit	7	6	5	4	3	2	1	0
Status High	0	0	SOT	SGIN	SBIN	SAIN	SDN	SUP

- SUP : Status counter up
- SDN : Status counter down
- SAIN : Status A Terminal Input
- SBIN : Status B Terminal Input
- SGIN : Status G Terminal Input
- SOT : Status Output Terminal (same as OT)

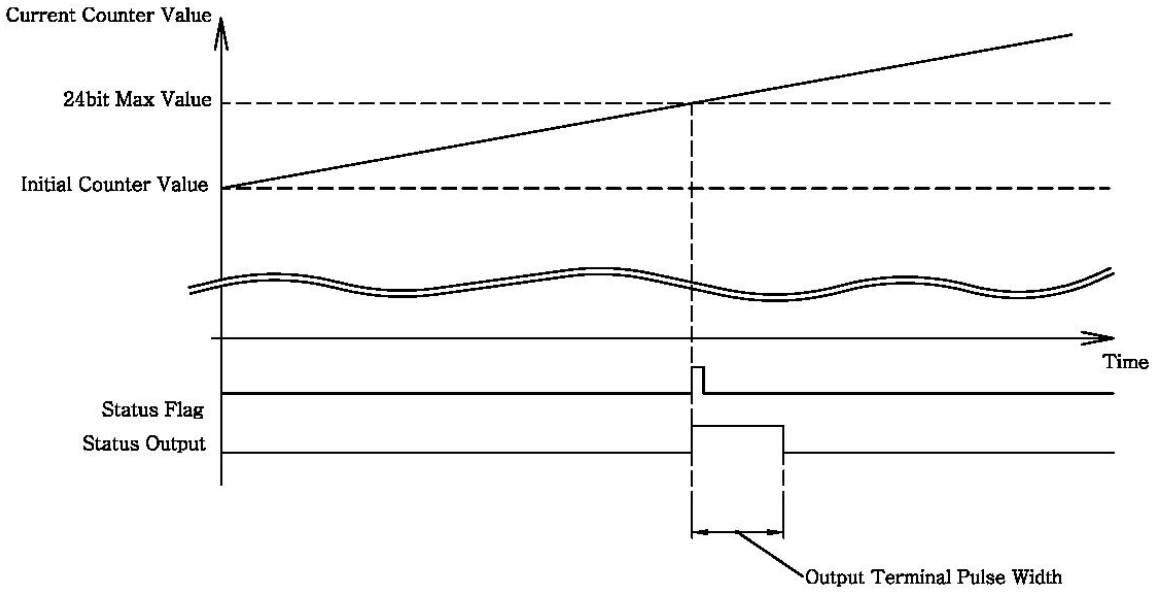
◆ Status Output Terminal(OT) Control

- This Status Output Terminal Control can read and write to binary.
- Summary of this register shows below table.

Decimal Bit							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status Output Terminal Selection				Status Output Terminal Pulse Widh			

Status Output Terminal Selection	Status Output Terminal Pulse Widh
“0000” : Force Off “0001” : GT “0010” : LT “0011” : EQ “0101” : Overflow “0110” : Underflow “1001” : Count Up “1010” : Count Down “1011” : A Terminal Input “1100” : B Terminal Input “1101” : G Terminal Input “1110” : PWM Output “1111” : Force On others : Force Off	“0000” : Bypass “0001” : 1msec “0010” : 5msec “0011” : 10msec “0100” : 20msec “0101” : 50msec “0110” : 100msec “0111” : 200msec “1000” : 500msec “1111” : Latched others : Bypass

Below example is output overflow flag in Status Register. When Status flag be the rising, Status Output Terminal Pulse Width be waiting by user setting value until.



◆ **Command or PWM duty value (PWM Output Mode)**

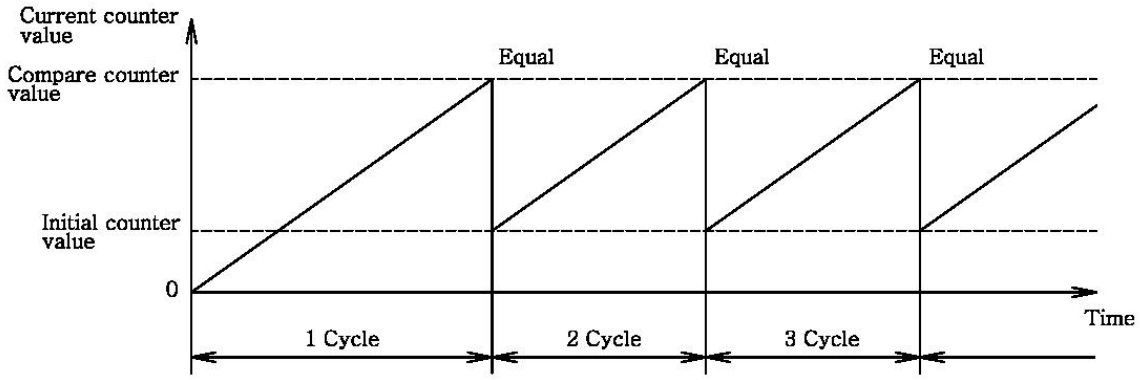
- This 1byte register can do use to Command or PWM duty value control. The Command control is used to general and if Gate Function/Counter Mode set to PWM Output Mode, this register is a variable of PWM output duty value.

- When used Command

- This register can control by user.
- This register used to reading and writing of binary number (8bit).
- Command shows bellows table.

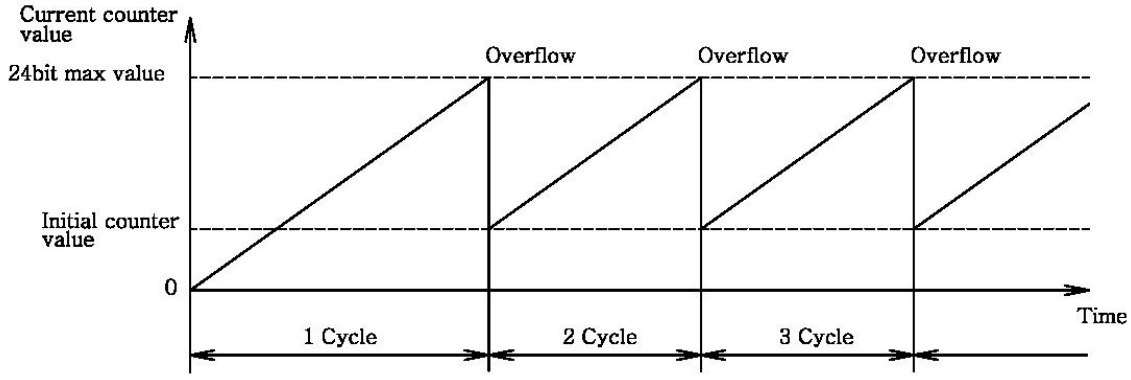
Bit	7	6	5	4	3	2	1	0
Command Register	HRST	CR	CP	CST	PU	PO	PE	IDS

- IDS : Input data selection (0 : Current counter value, 1 : Store counter value)
- PE : Process Equal
  - When Current counter value = Compare counter value, Current count value is setting to Initial counter value. Below example picture shows timing waveforms of Process Equal.



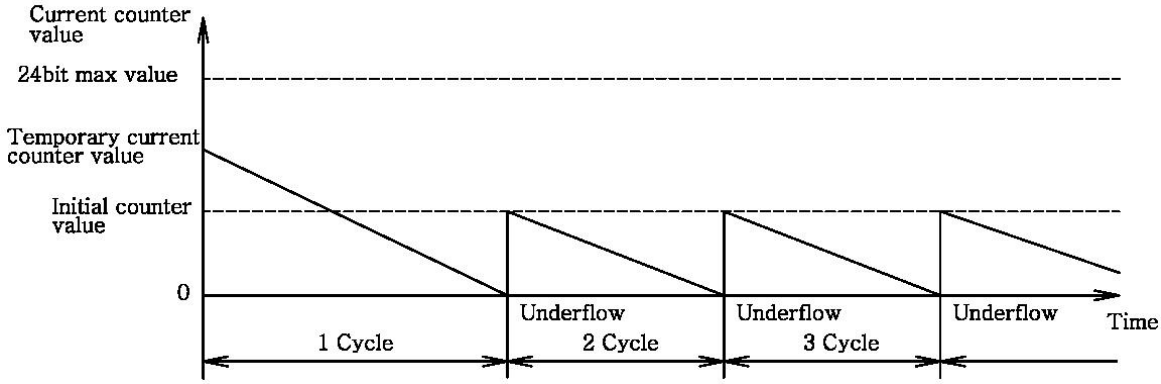
- PO : Process Underflow

- When Current counter value is overflow. Current count valueis setting to Initial counter value . Below example picture shows timing waveforms of Process Overflow.



- PU : Process Underflow

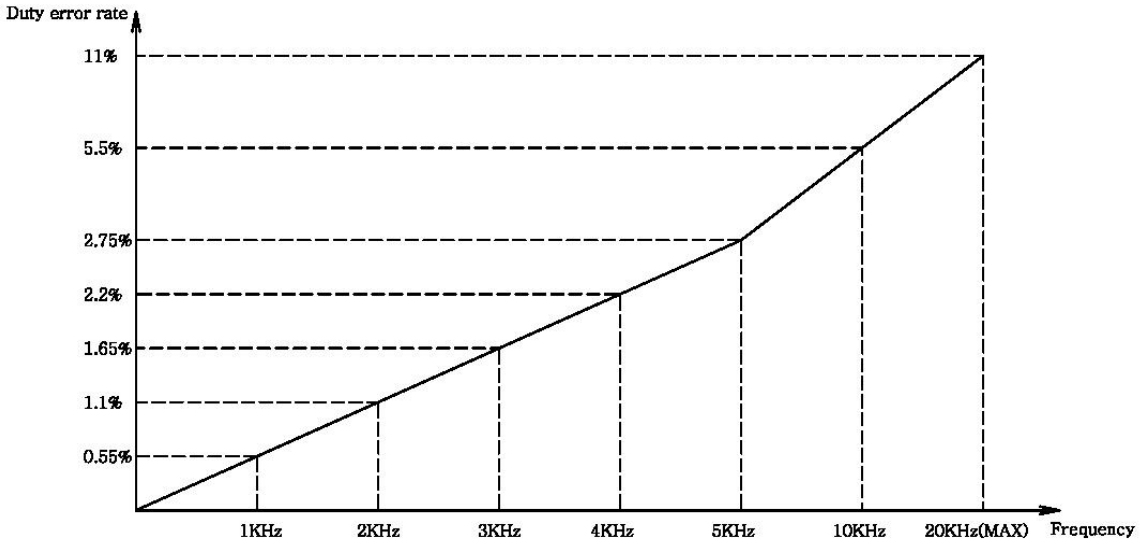
- When Current counter value is underflow, Current count values setting to Initial counter value. Below example picture shows timing waveforms of Process Underflow.



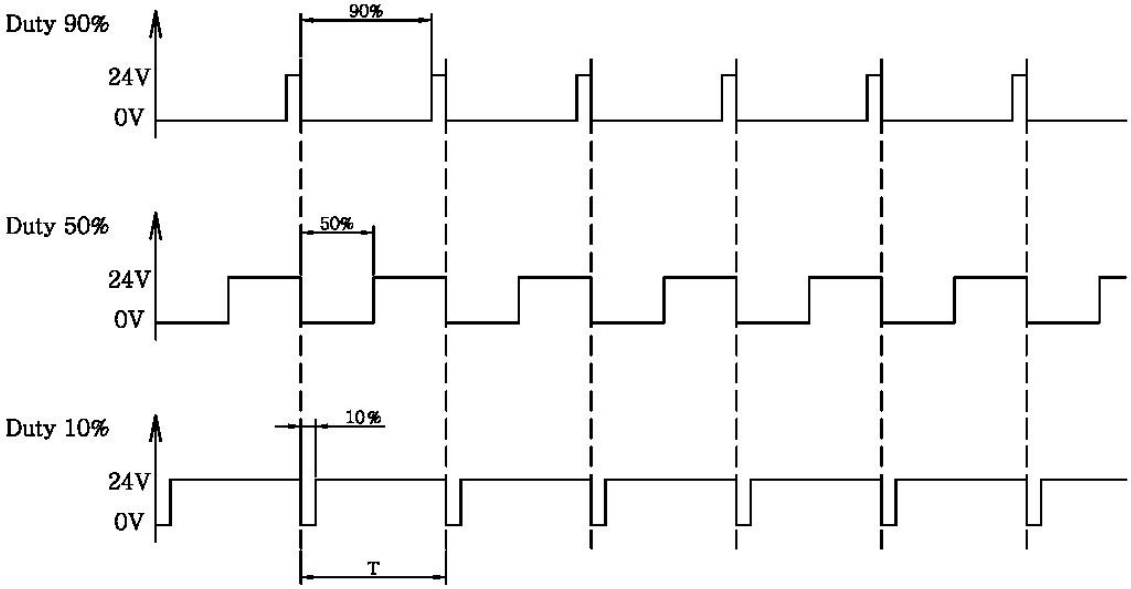
- CST : Clrar Status (SOT, SUF, SOF, SEQL)
- CP : Counter Preset, Current counter value = Initial counter value
- CR : Counter Reset, Current counter value = 0
- HRST : Reset current counter value, stored counter value and Stats

- When used PWM duty value

- When Counter Mode set to PWM Output Mode, this register can used to PWM duty value.
- PWM Duty = 0 ~ 100 (= 0 ~ 100%). If >100 then 100%.
- Below graphic is an error rate of duty(when Duty 50% and load 11KΩ).



- See the PWM Mode in Gate Function/Counter Mode
- Below example picture shows PWM waveforms about PWM duty value.



- T = Time (If Frequency = 10KHz then T= 0.1ms)

◆ **Gate Function/Counter Mode(Parameter Byte #0)**

- Counter Mode

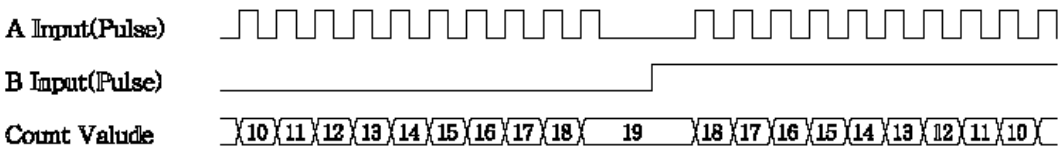
- 1 Pulse Mode (A : Pulse, B : Direction)

The 1 Pulse Mode reads incoming pulses and returns a binary number (0 to 16,777,215) to FnBus. The 1 Pulse Mode accepts only one-phase inputs. The module determines the Phase B input status to up or down count. (B Phase = High : Down Counter, B Phase = Low: Up Counter)

- Set Gate Function/Counter Mode (Parameter Byte#0) below table.

Bit	7	6	5	4	3	2	1	0
Counter Mode					0	0	0	1

- Below example picture shows timing waveforms of 1 Pulse Method Pulse Mode.



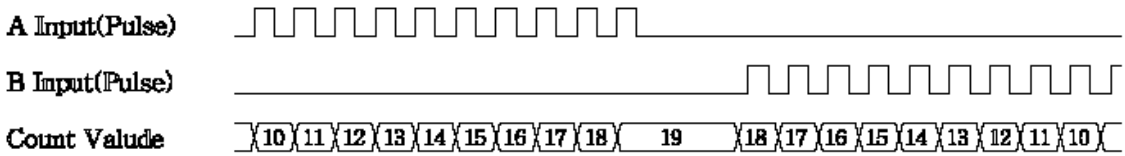
- 2 Pulse Mode (A : Up Pulse, B : Down Pulse)

The 2 Pulse Mode reads incoming pulses and returns a binary (0 to 16,777,215) to FnBus. The 2 Pulse Mode only accepts 2 Phase input. If A Phase reads incoming pulse and B Phase low, the time is up count state.

- Set Gate Function/Counter Mode (Parameter Byte#0) below table.

Bit	7	6	5	4	3	2	1	0
Counter Mode					0	0	1	0

- Below example picture shows timing waveforms of Pulse 2 Pulse Mode.

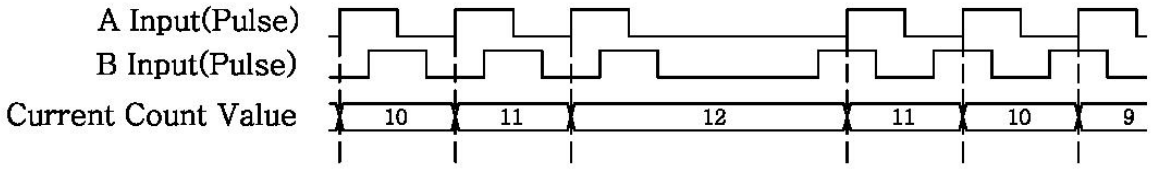


The Encoder x1 reads incoming pulse and returns number (0 to 16,777,215) to the FnBus. The Encoder x1 only accepts 2 Phase quadrature (90°) input. The mode senses the relationship between the 2 Phase, and counts up or down accordingly.

- Set Gate Function/Counter Mode (Parameter Byte#0) below table.

Bit	7	6	5	4	3	2	1	0
Counter Mode				Encoder x1.	0	0	1	1

- Below example picture shows timing waveforms of Encoder x1.



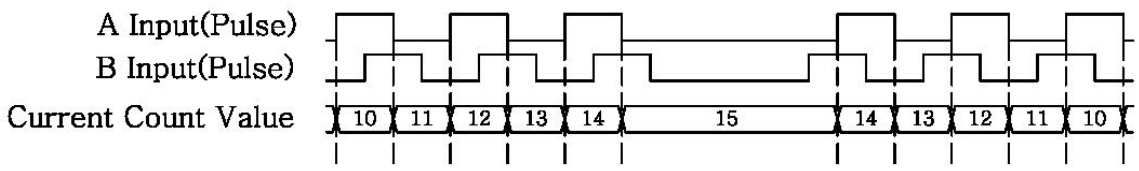
Encoder x2 (A/B ph, B/B ph)

The Encoder x2 reads incoming pulse and returns number (0 to 16,777,215) to the FnBus. The Encoder x2 only accepts 2 Phase quadrature (90°) input. The mode senses the relationship between the 2 Phase, and counts up or down accordingly.

- Set Gate Function/Counter Mode (Parameter Byte#0) below table.

Bit	7	6	5	4	3	2	1	0
Counter Mode				Encoder x2.	0	0	1	1

- Below example picture shows timing waveforms of Encoder x2.



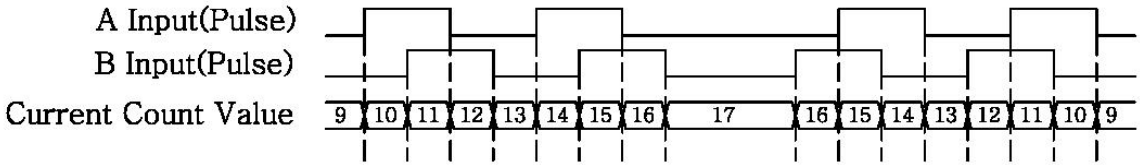
- Encoder x4 (A:Aph, B:Bph)

The Encoder x4 reads incoming pulse and returns number (0 to 16,777,215) to the FnBus. The Encoder x4 only accepts 2 Phase quadrature(90°) input. The mode senses the relationship between the 2 Phase, and counts up or down accordingly.

- Set Gate Function/Counter Mode (Parameter Byte#0) below table.

Bit	7	6	5	4	3	2	1	0
Counter Mode					0	1	0	1

- Below example picture shows timing waveforms of Encoder Mode x4.



- Period/Rate Mode (Gate Function Disabled)

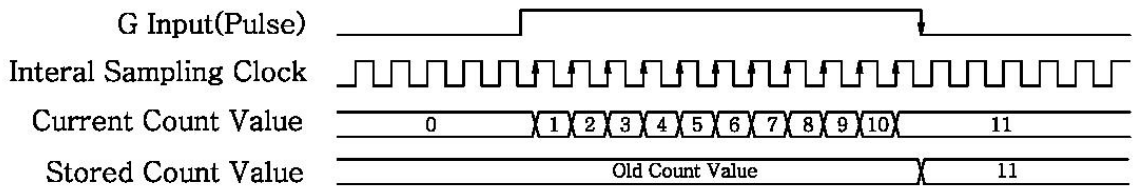
The Period/Rate Mode will return an incoming frequency and total Current Count Value to the FnBus, by gating an Internal Sampling Clock with an external signal.

This mode determines the frequency and total number of input pulses by incoming the number of internal sample clock over a user-specified number of input signal pulses. At the end of the specified number of pulses, the module returns the frequency. When the frequency is updated, both outputs are checked against their associated presets.

- Set the Gate Function/Counter Mode (Parameter Byte#0) with below table value that is Period/Rate Mode.

Bit	7	6	5	4	3	2	1	0
Counter Mode					0	1	1	0

- Below example picture shows timing waveforms of Period/Rate Mode.



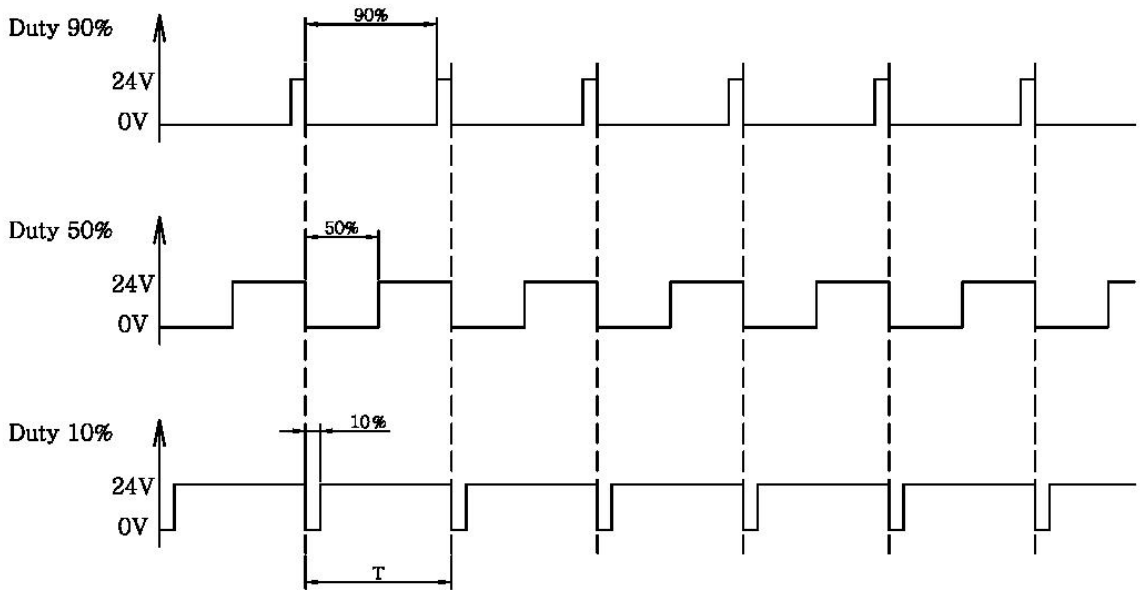
- PWM(Pulse Width Modulation) Output Mode

The PWM Output Mode uses the Current counter value to generate a continuous rolling sequence of numbers. The configurations of PWM range value have to a frequency(1 to 20Khz) and duty cycle (0 to 100%). The PWM output can be used to direct the PWMsignal to terminal output.

- Set the Gate Function/Counter Mode (Parameter Byte#0) with below table value that is PWM Output Mode.

Bit	7	6	5	4	3	2	1	0
Counter Mode					1	0	0	0

- Below example picture shows timing waveforms of PWM Output Mode.



- In above picture 'T' see "Setting PWM Frequency value" for frequency transform setting.
- See Command or PWM duty value for duty cycle setting
- See Status Output Terminal Control for terminal output setting.

- Gate Function Mode

This Gate Function will operate in one of five modes (Store/Continue, Store/Wait/Resume, Store-Reset/Wait/ and Store-Reset/Start). The Gate Function was unused to Period /Rate.

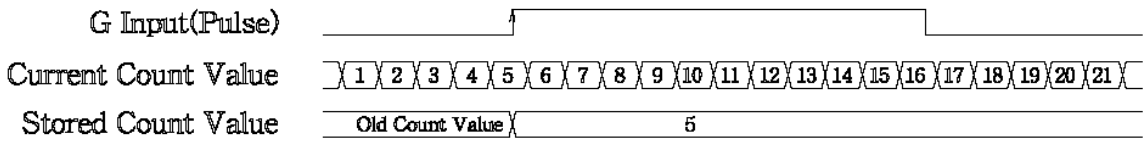
- Store/Continue

When G ph are rising edge, The Stored Count Value register will get counting value by Current Count Value register. Next Current Count Value will do counting continue.

- Set the Gate Function/Counter Mode (Parameter Byte#0) with below table value that is Store/Continue.

Bit	7	6	5	4	3	2	1	0
Counter Mode	0	0	0	1				

- Below example picture shows timing waveforms of Store/Continue.



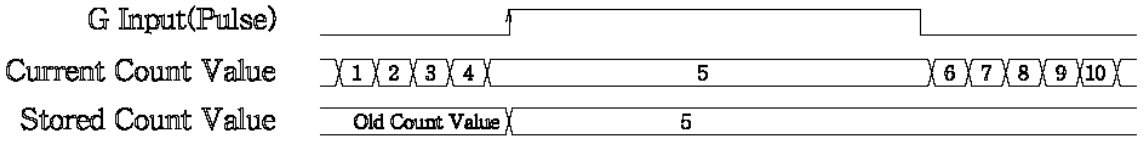
- Store/Wait/Resume

When G Ph are rising edge, The Stored Count Value register will get counting value by Current Count Value register and waits the Current Count Value until falling edge. Next G Phwill be filling edge and Current Count Value register resume counting.

- Set the Gate Function/Counter Mode (Parameter Byte#0) with below table value that is Store/Wait/Resume.

Bit	7	6	5	4	3	2	1	0
Counter Mode	0	0	1	0				

- Below example picture shows timing waveforms of Store/Wait/Resume.



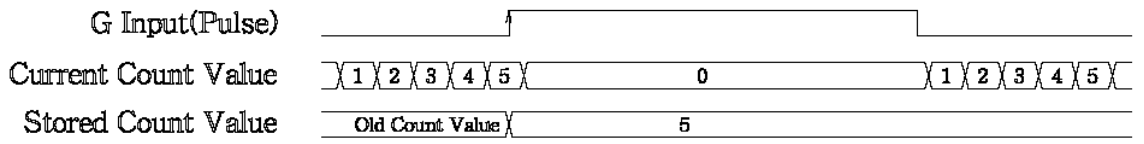
- Store-Reset/Wait/Start

When G Ph are rising edge, The Stored Count Value register will get counting value by Current Count Value register and Current Count Value register reset at the same time. The Current Count Value register wait until G Ph falling edge. Next Current Count Value register start counting.

- Set the Gate Function/Counter Mode (Parameter Byte#0) with below table value that is Store-Reset/Wait/Start.

Bit	7	6	5	4	3	2	1	0
Counter Mode	0	0	1	1				

- Below example picture shows timing waveforms of Store-Reset/Wait/Start.

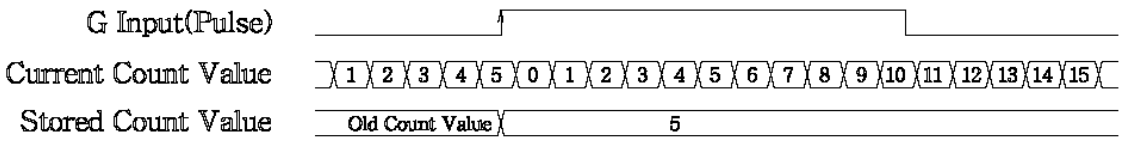


- **Store-Reset/Start**
  When G Ph are rising edge, The Stored Count Value register will get counting value by Current Count Value register and Current Count Value register reset at the same time and the register start counting.

- Set the Gate Function/Counter Mode (Parameter Byte#0) with below table value that is Store-Reset/Start.

Bit	7	6	5	4	3	2	1	0
Counter Mode	0	1	0	0				

- Below example picture shows timing waveforms of Store-Reset/Start.

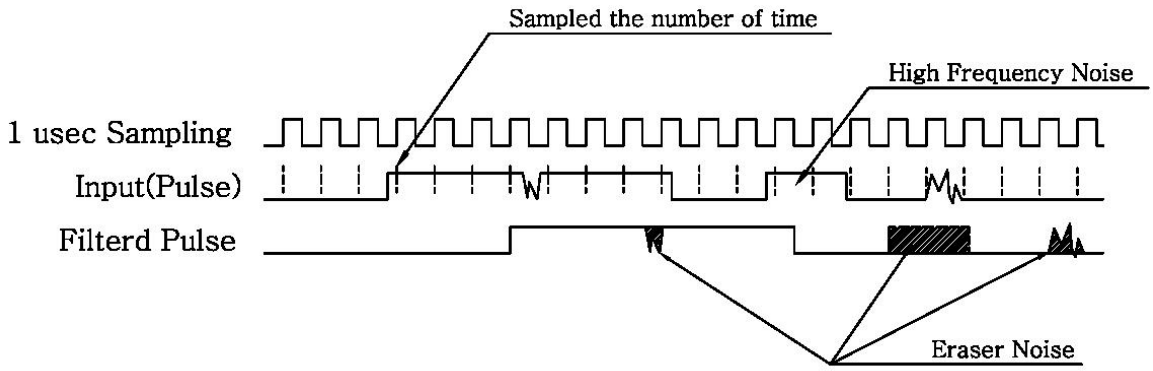


◆ Gate Sampling Time/Input Filter(Parameter Byte #1)

- This Gate Sampling Time/Input Filter can read and write to binary.
- Summary of this register shows below table.

Decimal Bit							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Gate Sampling Time				Input Filter			
“0000” : (10/1) Mhz (0.1us) “0001” : (10/2) Mhz (0.2us) “0010” : (10/4) Mhz (0.4us) “0011” : (10/8) Mhz (0.8us) “0100” : (10/16) Mhz (1.6us) “0101” : (10/32) Mhz (3.2us) “0110” : (10/64) Mhz (6.4us) “0111” : (10/128) Mhz (12.8us) others : (10/1) Mhz(0.1us)				“0000” : Bypass (about 1.5Mhz) “0001” : 1usec (500Khz ±30%) “0010” : 5usec (100Khz ±30%) “0011” : 10usec (50Khz ±30%) “0100” : 50usec (10Khz ±30%) “0101” : 100usec (5Khz ±30%) “0110” : 500usec (1000hz ±30%) “0111” : 1msec (500hz ±30%) “1000” : 5msec (100hz ±30%) “1001” : 10msec (50hz ±30%) others : Bypass (about 1.5Mhz)			

- FnIO-HSC-5101 module has low path filter which can control by Input Filter (0 to 4bit) value. When Input Filter is 1usec sampling, the filtering principle shows below picture. The sampled the number of time can third more. Otherwise Input pulse be erasing with below sample picture.If Input Filter is setting to 5usec("0010"), passing frequency is 0 ~ 100Hhz.



- When this register used to Period/Rate mode, Internal Sampling Clock set frequency.

◆ **Stored counter value Register**

- This register can only return to 24bit binary number (0 to 16,777,215).
- This register used to Period/Rate and Gate Counter mode.

◆ **Initial Counter Value**

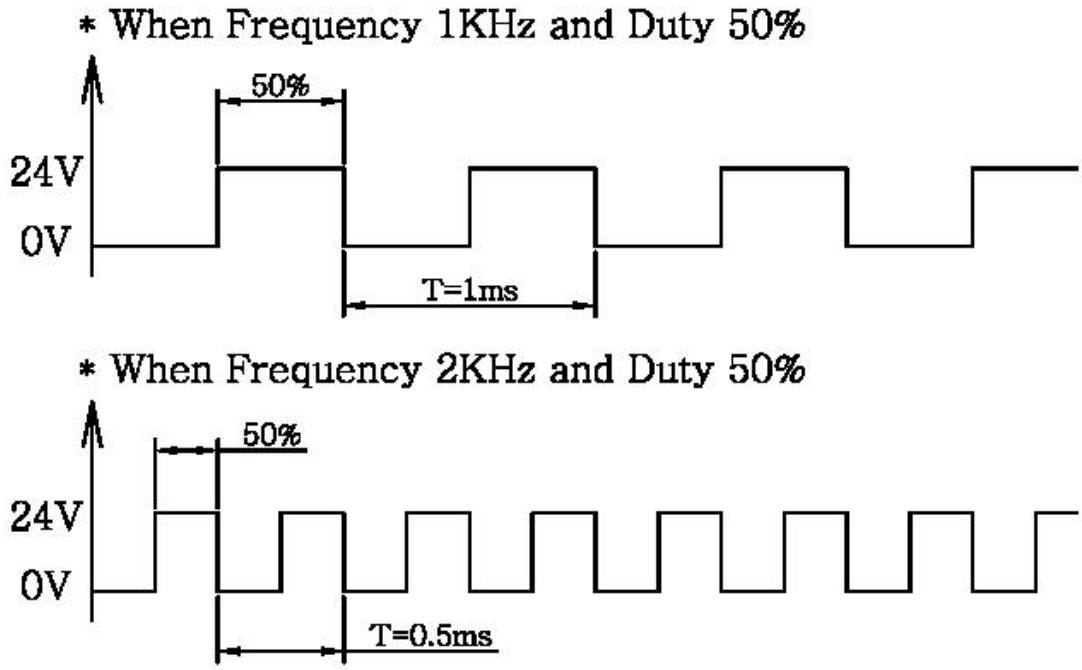
This 4byte register can do use to Initial counter or PWM Frequency value control. The Initial counter value is used to general configuration the Current counter value and if Gate Function/Counter Mode set to PWM Output Mode, this register is a variable of PWM output frequency value.

- General configuration for initial current counter

- FnIO HSC-5101 Module exist Initial counter value for starting of Current count value.
- Current count value begins starting from Initial counter value.
- User can configuration of Initial counter value.
- If user can' t configuration of Initial counter value, that is fixed to value (0x000000).
- This Initial counter value used to PO,PU and PE.
- This Initial counter value can reading and writing to binary number (0 to 16,777,215).

- Setting PWM Frequency value

- If Gate Function/Counter Mode set to PWM Output Mode, this register is frequency value of PWM output
- PWM Frequency = 1 ~ 20000 (=1Hz~20KHz). If PWM Frequency value< 1 then Off, if PW M Frequency value > 20000 then 20KHz
- Below example picture shows timing waveforms of PWM Output Mode.



◆ **Compare counter value**

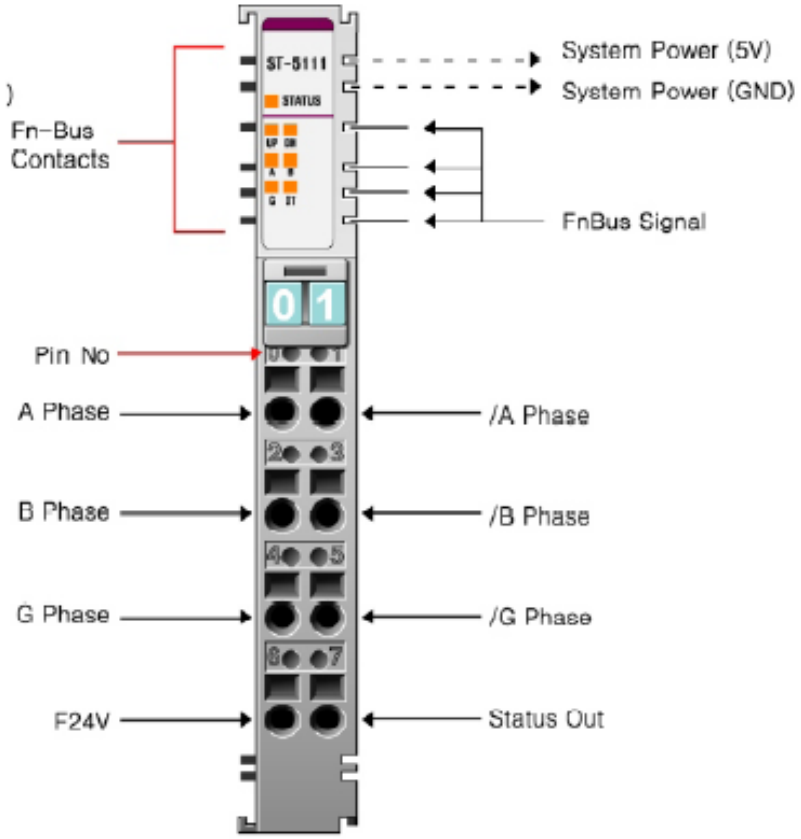
- In FnBus HSC-5101 Module exist Compare counter value for compare with Current Count Value.
- Status does transformation by compare value of Current Count Value and Compare Value Set Register.
- Compare counter value used to comparison Current Counter value for Status.
- If user can't configuration of Compare counter value, that is fixed to value (0x000000).
- This register use to PO,PU,PE and Status output.
- This register can reading and writing to binary number(0 to 16,777,215).

2) ST-5111

- 1 channel Incremental Encoder Interface Terminal Type

※ **Memory Register Map and Register Description are same with ST-5101**

◆ **Module View**



Mapping Data into the image table

◆ **I/O Process Image Table**

- Input Data

Byte Offset	Decimal Bit							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte #0	Current Count Value(Low) when IDS=0 Stored Count Value (Low) when IDS=1							
Byte #1	Current Count Value(Low) when IDS=0 Stored Count Value (Low) when IDS=1							
Byte #2	Current Count Value(Low) when IDS=0 Stored Count Value (Low) when IDS=1							
Byte #3	Always 0							
Byte #4	Status Low(Compared flags)							
	0	0	SUF	SOF	SEQL	SEQ	SLT(<)	SGT(>)
Byte #5	Status High(same as LED Display)							
	0	0	SOT	SGIN	SBIN	SAIN	SDN	SUP

- Output Data

<table>
<tr><th rowspan="2">Byte Offset</th><th colspan="8">Decimal Bit</th></tr>
<tr><th>Bit7</th><th>Bit6</th><th>Bit5</th><th>Bit4</th><th>Bit3</th><th>Bit2</th><th>Bit1</th><th>Bit0</th></tr>
<tr><td>Byte #0</td><td colspan="8">Output Terminal (OT) Control</td></tr>
<tr><td></td><td colspan="4">Output Terminal Selection
"0000" : Force Off
"0001" : GT
"0010" : LT
"0011" : EQ
"0101" : Overflow
"0110" : Underflow
"1001" : CountUp
"1010" : CountDown
"1011" : A Terminal Input
"1100" : B Terminal Input
"1101" : G Terminal Input
"1110" : PWM Output
"1111" : Force On
Others : Force Off</td><td colspan="4">Output Terminal Pulse Width
"0000" : Bypass
"0001" : 1msec
"0010" : 5msec
"0011" : 10msec
"0100" : 20msec
"0101" : 50msec
"0110" : 100msec
"0111" : 200msec
"1000" : 500msec
"1111" : Latched
Others : Bypass</td></tr>
<tr><td rowspan="3">Byte #1</td><td colspan="8">Command or PWM duty value (PWM Output Mode)</td></tr>
<tr><td rowspan="2">Command</td><td>Bit7</td><td>Bit6</td><td>Bit5</td><td>Bit4</td><td>Bit3</td><td>Bit2</td><td>Bit1</td><td>Bit0</td></tr>
<tr><td>HRST</td><td>CR</td><td>CP</td><td>CST</td><td>PU</td><td>PO</td><td>PE</td><td>IDS</td></tr>
<tr><td>PWM Duty value</td><td colspan="8">0~100dec (=0~100%)</td></tr>
</table>

◆ Input Data Byte #4

SUF : Status Underflow (Latched)
SOF : Status Overflow (Latched)
SEQL(=) : Status Current count value = Compare count value (Latched)
SEQ(=) : Status Current count value = Compare count value (Unlatched)
SLT(<) : Status Current count value < Compare count value (Unlatched)
SGT(>) : Status Current count value > Compare count value (Unlatched)

◆ Input Data Byte #5

SOT : Status Output Terminal (same as OT)
SGIN : Status G Terminal Input
SBIN : Status B Terminal Input
SAIN : Status A Terminal Input
SDN : Status Counter Down
SUP : Status Counter Up

◆ Output Data Byte #1

HRST : HSC Reset
CR : Counter Reset, Current count value=0
CP : Counter Preset, Current count value=Initial count value
CST : Clear Status (SOT,SUF,SOF,SEQL)
PO : Process Overflow
PU : Process Underflow

PE : Process Equal
IDS : Input Data Selection (0 : Current count value, 1 : Store count value)

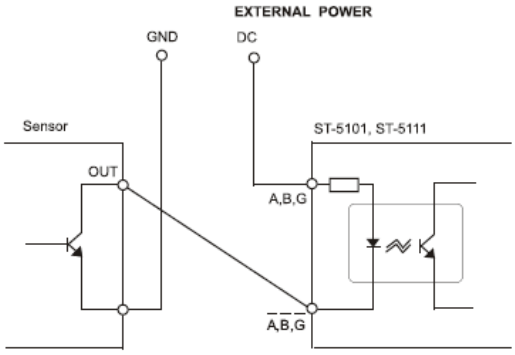
◆ Specification

Input Specification	
Input Voltage	24Vdc
Input Current	6.1mA@24Vdc
Input On-State Current	Input Current≥2.9mA
Input On-State Voltage	Input Voltage≥12Vdc
Output On-State Current	Input Current≤0.15mA
Output On-State Voltage	Input Voltage≤1.8Vdc
Max. On-State Voltage	30V
Max. Input Frequency	Max. 1.5MHz
Input filter selections	Bypass, 1㎲, 5㎲, 10㎲, 50㎲, 100㎲, 500㎲, 1㎳, 5㎳, 10㎳
Number of Inputs	0-1 group of A and /A (or GND) 2-3 group of B and /B (or GND) 4-5 group of G and /G (or GND)
Output Specification	
Number Of Output	6-7 States Output
Output Control	Output and be tied to any of 13State
Output Supply Voltage Range	5 to 28.8Vdc (HSC Status Output)
On State Current	Max. 1mA
Output Signal Delay	OFF to ON : Max. 0.5ms ON to OFF : Max. 1ms
Output Current Rating	Max. 0.5A
Output Type	Sink Type
Over Current Protection	1.8A (Shutdown Current)
Module Specification	
Power Dissipation	Max. 80mA @ 5.0Vdc
Isolation	I/O to Logic : Photo-coupler Isolation
	Field Power : Not Connected
Weight	70g
Size	12mm × 99mm × 70mm

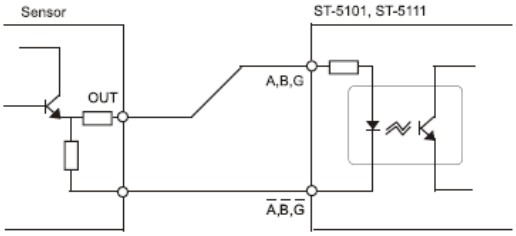
◆ Wiring Description

Pin No.	Description	Pin No.	Description
0	A Pulse Input	1	/A Pulse Input
2	B Pulse Input	3	/B Pulse Input
4	G Pulse Input	5	/G Pulse Input
6	F24V	7	Status Output(Sink)

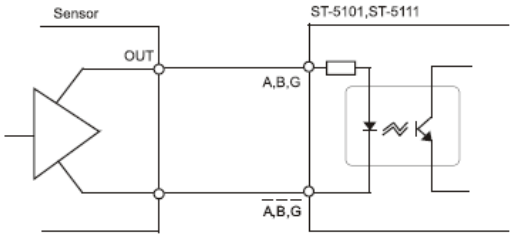
(1) Open Collector



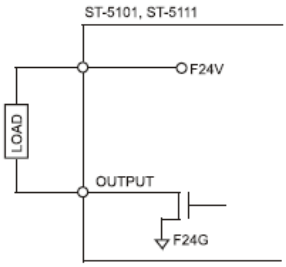
(2) VOLTAGE OUTPUT



(3) LINE DRIVE



(4) SINK OUTPUT (STATUS)



◆ **Configuration Parameter Table**

Offset	Access						Description
Byte#0	R/W	00-03	3	2	1	0	Counter Mode
			0	0	0	0	Counter Disabled
			0	0	0	1	1Pulse Mode (A:Pulse, B:Direction)
			0	0	1	0	2Pulse Mode (A:UpPulse, B:DownPulse)
			0	0	1	1	Encoder x1 (A:Aph B:Bph)
			0	1	0	0	Encoder x2 (A:Aph B:Bph)
			0	1	0	1	Encoder x4 (A:Aph B:Bph)
			0	1	1	0	Period/Rate Mode (Gate Function Disabled)
			0	1	1	1	Reserved
			1	0	0	0	PWM Output Mode (Gate Function Disabled)
			1	0	0	1	Reserved
			Others				Counter Disabled
		04-07	7	6	5	4	Gate Function
			0	0	0	0	Gate Function Disable
			0	0	0	1	Store/Continue
			0	0	1	0	Store/Wait/Resume
			0	0	1	1	Store-Reset/Wait/Start
			0	1	0	0	Store-Reset/Start
			Others				Gate Function Disabled
Byte#1		00-03	3	2	1	0	Input Filter
			0	0	0	0	Bypass (about 1.5㎒)
			0	0	0	1	1㎲±40%
			0	0	1	0	5㎲±40%
			0	0	1	1	10㎲±40%
			0	1	0	0	50㎲±40%
			0	1	0	1	100㎲±40%
			0	1	1	0	500㎲±40%
			0	1	1	1	1㎳±40%
			1	0	0	0	5㎳±40%
			1	0	0	1	10㎳±40%
			Others				Bypass (about 1.5㎒)
		04-07	7	6	5	4	Gate Sampling Time
			0	0	0	0	(10/1)㎒ (0.1㎲)
			0	0	0	1	(10/2)㎒ (0.2㎲)
			0	0	1	0	(10/4)㎒ (0.4㎲)
			0	0	1	1	(10/8)㎒ (0.8㎲)
			0	1	0	0	(10/16)㎒ (1.6㎲)
			0	1	0	1	(10/32)㎒ (3.2㎲)
			0	1	1	0	(10/64)㎒ (6.41㎲)
			0	1	1	1	(10/128)㎒ (12.8㎲)
			Others				(10/1)㎒ (0.1㎲)

3. Serial Interface Module

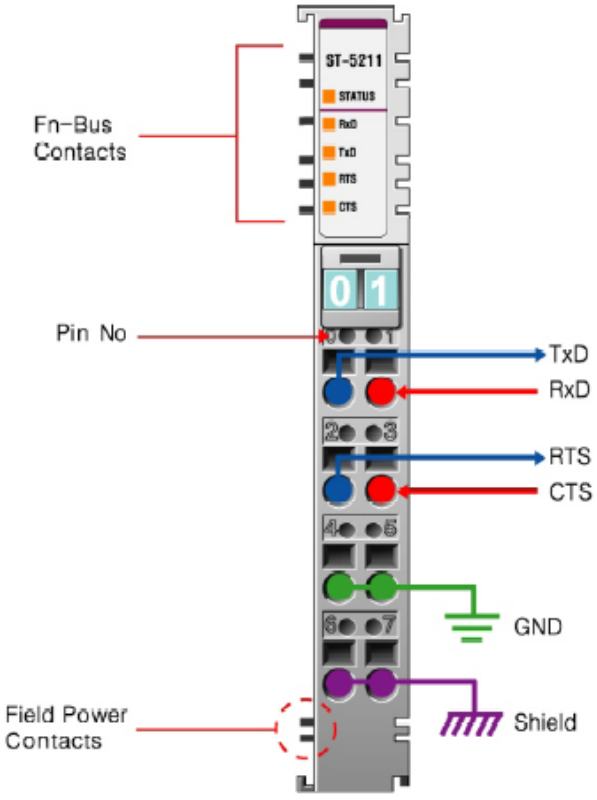
Description

- ST-52xx series is Serial Interface module.
- It supports 300bps~115.2Kbps for the communication speed .
- It has 3~5 LEDs for Status indication. One indicates Module Status, the others indicate communication status.
- It is isolated between Field I/O and FnBus by using Photo-coupler.
- It is operated regardless of Field Power supply. When the supplied Field Power has changed, the Expansion Field Power Supply(ST-7241) is required absolutely to be used.

1) ST-5211

- 1Channel Serial Interface RS-232 Terminal Type

◆ **Module View**



Mapping Data into the image table

◆ **I/O Process Image Table**

- Input Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
Byte#1	Data Byte#0								
Byte#2	Data Byte#1								
Byte#3	Data Byte#2								
Byte#4	Data Byte#3								
Byte#5	Data Byte#4								

- Output Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Control Byte	TPR	OL2	OL1	OL0	-	RA	TR	IR
Byte#1	Data Byte#0								
Byte#2	Data Byte#1								
Byte#3	Data Byte#2								
Byte#4	Data Byte#3								
Byte#5	Data Byte#4								

- Status Byte

- IA : Initialization Acknowledge
- TA : Transmit Acknowledge
- RR : Receive Request
- RBO : RxD Buffer Overrun Error

There are two counters (Run counter and Index Counter) which pointing at the position of RxD Buffer. Run counter is increased +1 whenever RxD input, Index counter is increased as much as Input length that brought on Input data.

Therefore, if (Run counter - Index counter)>1024(RxD Buffer Size), RxD Buffer Overrun error occurs.

- IL0~IL2 : Input length
- TPA : Transmit Processing Acknowledge

(Related Configuration Parameter:TxD Buffering)

- Control Byte

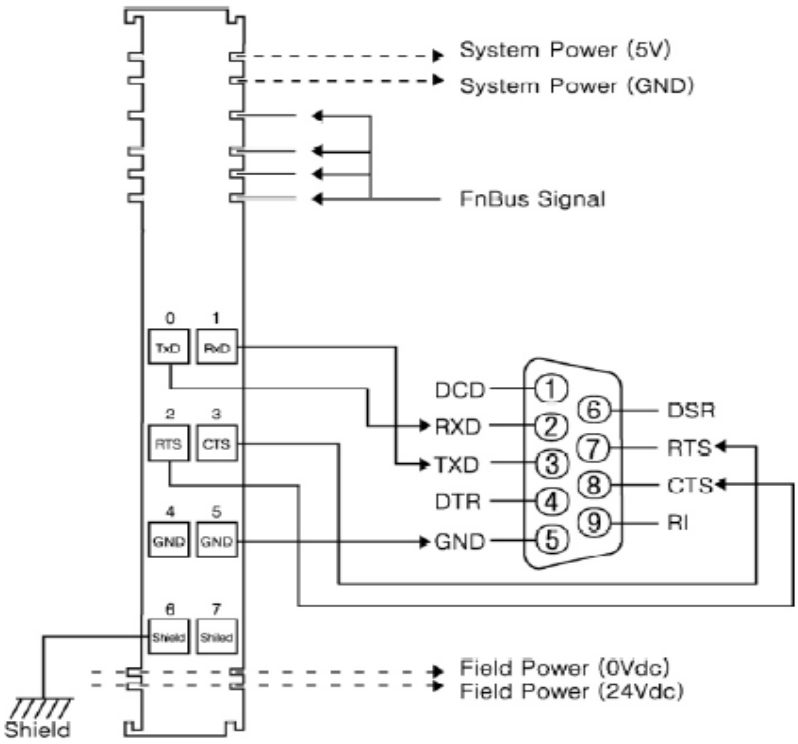
- IR : Initialization Request
- TR : Transmit Request
- RA : Receive Acknowledge
- OL0~OL2 : Output Length
- TRR : Transmit Processing Request

(Related Configuration Parameter : TxD Buffering)

◆ Specification

Input Specification	
Transfer Channels	TxD, RxD, Full Duplex
Transfer Rate	300~115200bps
Data Bit	7bit, 8bit, 9bit
Parity Bit	None, Odd, Even
Stop Bit	1bit, 2bit
Flow Control	RTS, CTS
Bit Distortion	<1.6%
Connection	Spring force of RTB
Cable Length	Max. 15m
Low Signal Voltage	-18V ~ -3V
High Signal Voltage	3V ~ 18V
Data Buffer	In/Out User Data 5Bytes, Control/Status 1byte
RxD Buffer	1024bytes
TxD Buffer	256bytes
Input Image Size	6bytes
Output Image Size	6bytes
Module Specification	
Power Dissipation	Max. 95mA @ 5.0Vdc
Isolation	Photo-coupler Isolation, Isolation Voltage:1000Vrms/Vac
Size	12mm × 99mm × 70mm

◆ Module Wire Diagram



- Wiring Description

Pin No.	Description	Pin No.	Description
0	TxD	1	RxD
2	RTS	3	CTS
4	GND	5	GND
6	Shield	7	Shield

◆ Configuration Parameter Table

Offset	Decimal Bit							
Byte#0	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2it**	**1Bit**	**0it**
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Other : Unused *Default : 00		Data Bit 00 : 7Data bit 01 : 8Data bit 10 : 9Data bit Other : Unused *Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010 : 2400bps 0011 : 4800bps 0100 : 9600bps (*Default Value) 0101 : 19200bps 0110 : 38400bps 0111 : 57600bps 1000 : 115200bps Other : Unused			
Byte#1	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved				CTS/RTS Flow Control 00 : RTS/CTS Disable 01 : RTS Enable 10 : CTS Enable 11 : RTS/CTS Enable Default : 00 Note 1		TxD Process 0:Disable 1:Enable Default:0 Note 2	Stop BIt 0 : 1bit 1 : 2bit Default : 0
Byte#2	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved							
Byte#3	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved							

- Note 1

When RTS Enable, if size of received Data is bigger then 80%(1024*0.8=819) of RxD Buffer size, RTS output actives

- Note 2

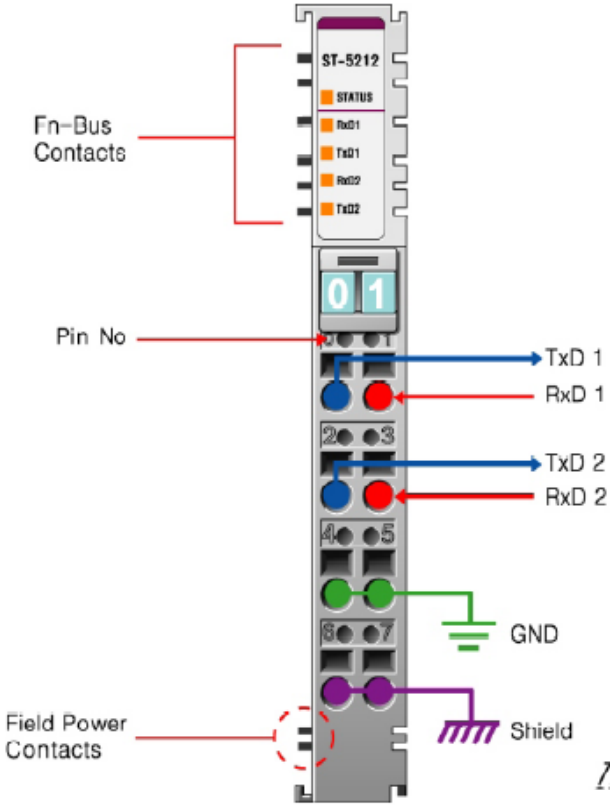
Disable : Transmit immediately Output Data #0 ~ Output Data #4

Enable : Store the value of Output Data continually at RxD Buffer of Serial Interface Module When TPA bit and TPR bit of Control Byte and Status Byte are different, transmit all Data that saved at TxD Buffer

2) ST-5212

- 2 Channel Serial Interface RS-232 Terminal Type

◆ Module View



Mapping Data into the image table

◆ I/O Process Image Table

- Input Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Status Byte(1CH)	TPA	IL2	IL1	IL0	OR	RR	TA	IA
Byte#1	Data Byte#0(1CH)								
Byte#2	Data Byte#1(1CH)								
Byte#3	Data Byte#2(1CH)								
Byte#4	Data Byte#3(1CH)								
Byte#5	Data Byte#4(1CH)								
Byte#0	Status Byte(2CH)	TPA	IL2	IL1	IL0	OR	RR	TA	IA
Byte#1	Data Byte#0(2CH)								
Byte#2	Data Byte#1(2CH)								
Byte#3	Data Byte#2(2CH)								
Byte#4	Data Byte#3(2CH)								
Byte#5	Data Byte#4(2CH)								

- Output Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Control Byte(1CH)	TPR	OL2	OL1	OL0	-	RA	TR	IR
Byte#1	Data Byte#0(1CH)								
Byte#2	Data Byte#1(1CH)								
Byte#3	Data Byte#2(1CH)								
Byte#4	Data Byte#3(1CH)								
Byte#5	Data Byte#4(1CH)								
Byte#0	Control Byte(2CH)	TPR	OL2	OL1	OL0	-	RA	TR	IR
Byte#1	Data Byte#0(2CH)								
Byte#2	Data Byte#1(2CH)								
Byte#3	Data Byte#2(2CH)								
Byte#4	Data Byte#3(2CH)								
Byte#5	Data Byte#4(2CH)								

- Status Byte

- IA : Initialization Acknowledge
- TA : Transmit Acknowledge
- RR : Receive Request
- RBO : RxD Buffer Overrun Error
  There are two counters (Run counter and Index Counter) which pointing at the position of RxD Buffer. Run counter is increased +1 whenever RxD input, Index counter is increased as much as Input length that brought on Input data.
  Therefore, if (Run counter - Index counter)>1024(RxD Buffer Size), RxD Buffer Overrun error occurs.
- IL0~IL2 : Input length
- TPA : Transmit Processing Acknowledge
  (Related Configuration Parameter : TxD Buffering)

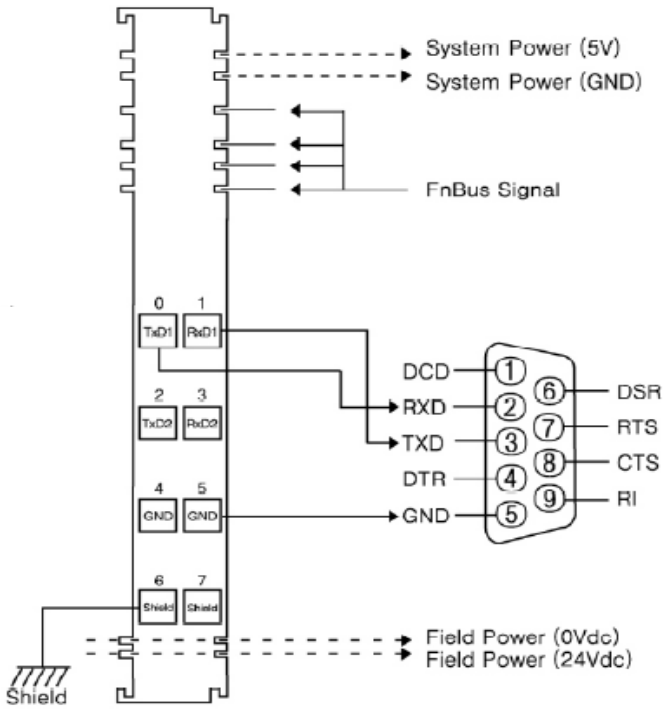
- Control Byte

- IR : Initialization Request
- TR : Transmit Request
- RA : Receive Acknowledge
- OL0~OL2 : Output Length
- TRR : Transmit Processing Request
  (Related Configuration Parameter : TxD Buffering)

◆ Specification

Input Specification	
Transfer Channels	TxD, RxD, Full Duplex
Transfer Rate	300~115200bps
Data Bit	7bit, 8bit, 9bit
Parity Bit	None, Odd, Even
Stop Bit	1bit, 2bit
Bit Distortion	<1.6%
Connection	Spring force of RTB
Cable Length	Max. 15m
Low Signal Voltage	-18V ~ -3V
High Signal Voltage	3V ~ 18V
Data Buffer	In/Out User Data 10Bytes, Control/Status 2byte
RxD Buffer	1024bytes
TxD Buffer	256bytes
Input Image Size	12bytes
Output Image Size	12bytes
Module Specification	
Power Dissipation	Max. 95mA @ 5.0Vdc
Isolation	Photo-coupler Isolation, Isolation Voltage : 1000Vrms/Vac
Size	12mm × 99mm × 70mm

◆ Module Wire Diagram



- Wiring Description

Pin No.	Description	Pin No.	Description
0	TxD1	1	RxD1
2	TxD2	3	RxD2
4	GND	5	GND
6	Shield	7	Shield

◆ Configuration Parameter Table

Offset	Decimal Bit							
Byte#0	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2it**	**1Bit**	**0it**
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Other : Unused *Default : 00		Data Bit 00 : 7Data bit 01 : 8Data bit 10 : 9Data bit Other : Unused *Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010 : 2400bps 0011 : 4800bps 0100 : 9600bps(*Default Value) 0101 : 19200bps 0110 : 38400bps 0111 : 57600bps 1000 : 115200bps Other : Unused			
Byte#1	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved						TxD Process 0:Disable 1:Enable *Default:0 *Note 1	Stop BIt 0 : 1bit 1 : 2bit Default : 0
Byte#2	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Other : Unused Default : 00		Data Bit 00 : 7Data bit 01 : 8Data bit 10 : 9Data bit Other : Unused Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010 : 2400bps 0011 : 4800bps 0100 : 9600bps (Default Value) 0101 : 19200bps 0110 : 38400bps 0111 : 57600bps 1000 : 115200bps Other : Unused			
Byte#3	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved						TxD Process 0:Disable 1:Enable *Default:0 *Note 1	Stop BIt 0 : 1bit 1 : 2bit Default : 0

*Note 1

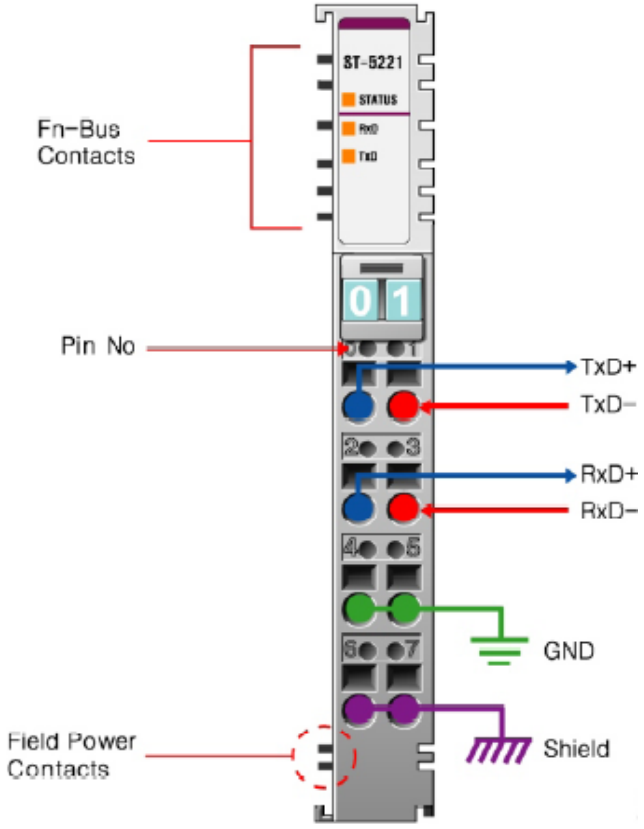
Disable : Transmit immediately Output Data #0 ~ Output Data #4

Enable : Store the value of Output Data continually at RxD Buffer of Serial Interface Module When TPA bit and TPR bit of Control Byte and Status Byte are different, transmit all Data that saved at TxD Buffer

3) ST-5221

- 1 Channel Serial Interface RS-422 Terminal Type

◆ **Module View**



Mapping Data into the image table

◆ **I/O Process Image Table**

- Input Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
Byte#1	Data Byte#0								
Byte#2	Data Byte#1								
Byte#3	Data Byte#2								
Byte#4	Data Byte#3								
Byte#5	Data Byte#4								

- Output Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Control Byte	TPR	OL2	OL1	OL0	-	RA	TR	IR
Byte#1	Data Byte#0								
Byte#2	Data Byte#1								
Byte#3	Data Byte#2								
Byte#4	Data Byte#3								
Byte#5	Data Byte#4								

- Status Byte

- IA : Initialization Acknowledge
- TA : Transmit Acknowledge
- RR : Receive Request
- RBO : RxD Buffer Overrun Error
  There are two counters (Run counter and Index Counter) which pointing at the position of RxD Buffer. Run counter is increased +1 whenever RxD input, Index counter is increased as much as Input length that brought on Input data.
  Therefore, if (Run counter - Index counter)>1024(RxD Buffer Size), RxD Buffer Overrun error occurs.
- IL0~IL2 : Input length
- TPA : Transmit Processing Acknowledge
  (Related Configuration Parameter : TxD Buffering)

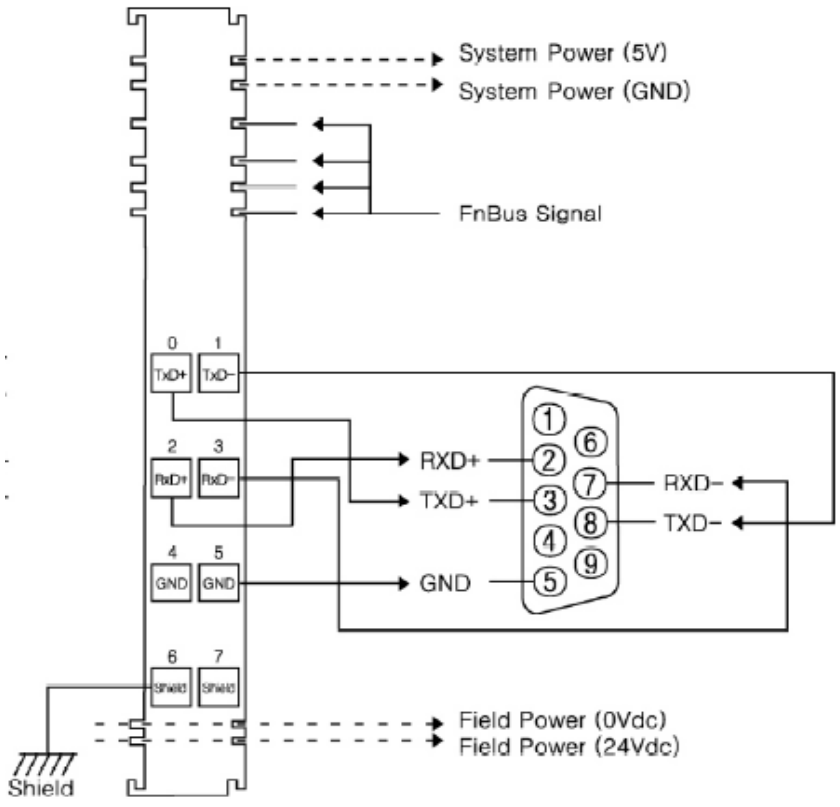
- Control Byte

- IR : Initialization Request
- TR : Transmit Request
- RA : Receive Acknowledge
- OL0~OL2 : Output Length
- TRR : Transmit Processing Request
  (Related Configuration Parameter : TxD Buffering)

◆ Specification

Input Specification	
Transfer Channels	TxD, RxD, Full Duplex
Transfer Rate	300~115200bps
Data Bit	7bit, 8bit, 9bit
Parity Bit	None, Odd, Even
Stop Bit	1bit, 2bit
Bit Distortion	<1.6%
Connection	Spring force of RTB
Cable Length	1㎞ twisted pair
Line Impedance	120ohm
Data Buffer	In/Out User Data 5Bytes, Control/Status 1byte
RxD Buffer	1024bytes
TxD Buffer	256bytes
Input Image Size	6bytes
Output Image Size	6bytes
Module Specification	
Power Dissipation	Max. 155mA @ 5.0Vdc
Isolation	Photo-coupler Isolation, Isolation Voltage : 1000Vrms/Vac
Size	12mm × 99mm × 70mm

◆ Module Wire Diagram



- Wiring Description

Pin No.	Description	Pin No.	Description
0	TxD+	1	TxD-
2	RxD+	3	RxD-
4	GND	5	GND
6	Shield	7	Shield

◆ Configuration Parameter Table

Offset	Decimal Bit							
Byte#0	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2it**	**1Bit**	**0it**
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Other : Unused Default : 00		Data Bit 00 : 7Data bit 01 : 8Data bit 10 : 9Data bit Other : Unused Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010 : 2400bps 0011 : 4800bps 0100 : 9600bps (Default Value) 0101 : 19200bps 0110 : 38400bps 0111 : 57600bps 1000 : 115200bps Other : Unused			
Byte#1	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved				CTS/RTS Flow Control 00 : RTS/CTS Disable 01 : RTS Enable 10 : CTS Enable 11 : RTS/CTS Enable Default:00 Note 1		TxD Process 0:Disable 1:Enable *Default:0 *Note 1	Stop Blt 0 : 1bit 1 : 2bit Default : 0
Byte#2	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved							
Byte#3	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved							

Note 1

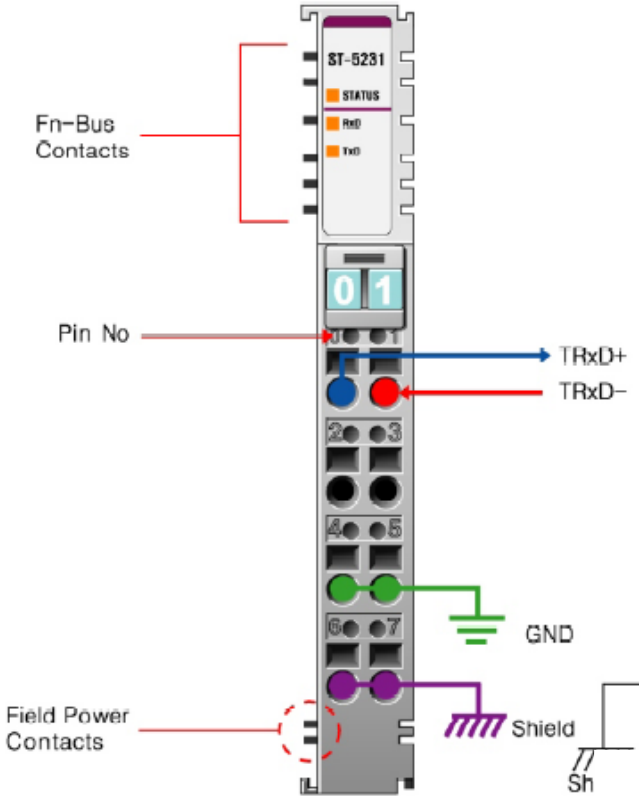
Disable : Transmit immediately Output Data #0~ Output Data #4

Enable : Store the value of Output Data continually at RxD Buffer of Serial Interface Module When TPA bit and TPR bit of Control Byte and Status Byte are different, transmit all Data that saved at TxD Buffer

4) ST-5231

- 1Channel Serial Interface RS-485 Terminal Type

◆ Module View



Mapping Data into the image t

◆ I/O Process Image Table

- Input Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
Byte#1	Data Byte#0								
Byte#2	Data Byte#1								
Byte#3	Data Byte#2								
Byte#4	Data Byte#3								
Byte#5	Data Byte#4								

- Output Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Control Byte	TPR	OL2	OL1	OL0	-	RA	TR	IR
Byte#1	Data Byte#0								
Byte#2	Data Byte#1								
Byte#3	Data Byte#2								
Byte#4	Data Byte#3								
Byte#5	Data Byte#4								

- Status Byte

- IA : Initialization Acknowledge
- TA : Transmit Acknowledge
- RR : Receive Request
- RBO : RxD Buffer Overrun Error

There are two counters (Run counter and Index Counter) which pointing at the position of RxD Buffer. Run counter is increased +1 whenever RxD input, Index counter is increased as much as Input length that brought on Input data.

Therefore, if (Run counter - Index counter)>1024(RxD Buffer Size), RxD Buffer Overrun error occurs.

- IL0~IL2 : Input length
- TPA : Transmit Processing Acknowledge
  (Related Configuration Parameter : TxD Buffering)

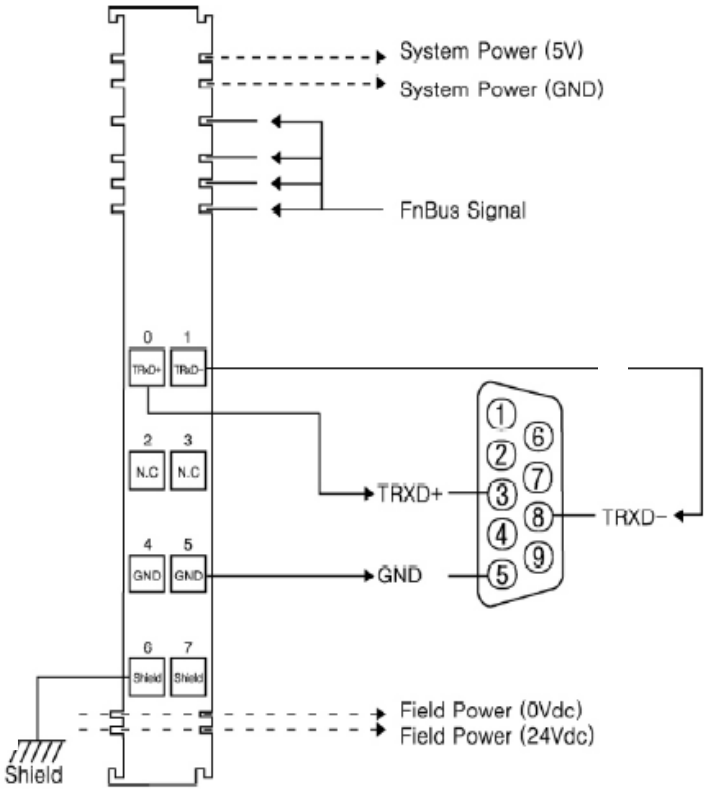
- Control Byte

- IR : Initialization Request
- TR : Transmit Request
- RA : Receive Acknowledge
- OL0~OL2 : Output Length
- TRR : Transmit Processing Request
  (Related Configuration Parameter : TxD Buffering)

◆ Specification

Input Specification	
Transfer Channels	TxD, RxD, Half Duplex
Transfer Rate	300~115200bps
Data Bit	7bit, 8bit, 9bit
Parity Bit	None, Odd, Even
Stop Bit	1bit, 2bit
Bit Distortion	<1.6%
Connection	Spring force of RTB
Cable Length	1㎞ twisted pair
Line Impedance	120ohm
Data Buffer	In/Out User Data 5Bytes, Control/Status 1byte
RxD Buffer	1024bytes
TxD Buffer	256bytes
Input Image Size	6bytes
Output Image Size	6bytes
Module Specification	
Power Dissipation	Max. 150mA @ 5.0Vdc
Isolation	Photo-coupler Isolation, Isolation Voltage : 1000Vrms/Vac
Size	12mm × 99mm × 70mm

◆ Module Wire Diagram



- Wiring Description

Pin No.	Description	Pin No.	Description
0	TRxD+	1	TRxD-
2	N.C	3	N.C
4	GND	5	GND
6	Shield	7	Shield

◆ Configuration Parameter Table

Offset	Decimal Bit							
Byte#0	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2it**	**1Bit**	**0it**
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Other : Unused Default : 00		Data Bit 00 : 7Data bit 01 : 8Data bit 10 : 9Data bit Other : Unused Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010 : 2400bps 0011 : 4800bps 0100 : 9600bps (Default Value) 0101 : 19200bps 0110 : 38400bps 0111 : 57600bps 1000 : 115200bps Other : Unused			
Byte#1	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved				CTS/RTS Flow Control 00 : RTS/CTS Disable 01 : RTS Enable 10 : CTS Enable 11 : RTS/CTS Enable Default : 00 Note 1		TxD Process 0:Disable 1:Enable Default:0 Note 1	Stop BIt 0 : 1bit 1 : 2bit Default : 0
Byte#2	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved							
Byte#3	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved							

*Note 1

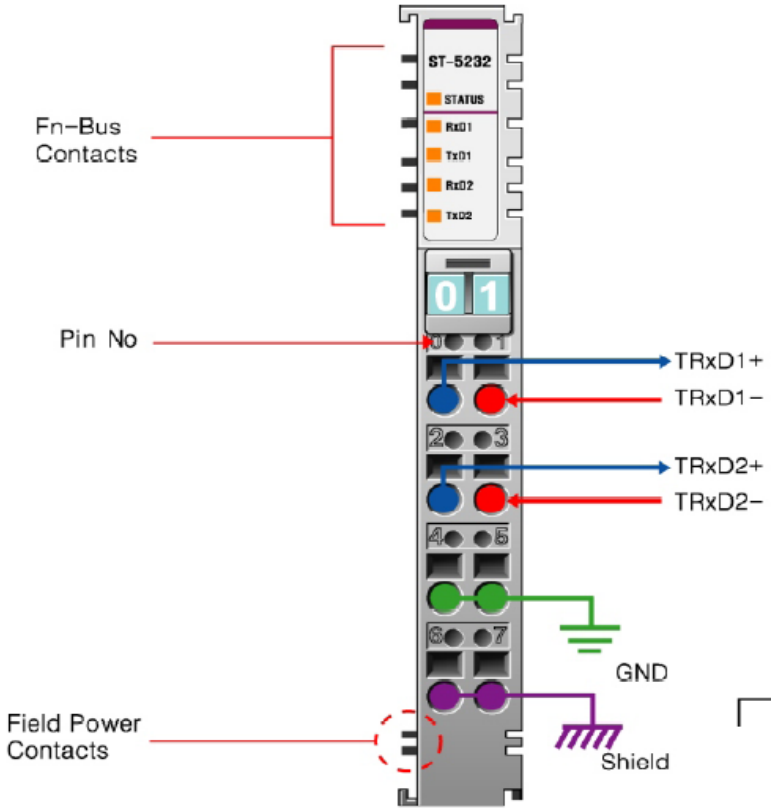
Disable : Transmit immediately Output Data #0~ Output Data #4

Enable : Store the value of Output Data continually at RxD Buffer of Serial Interface Module When TPA bit and TPR bit of Control Byte and Status Byte are different, transmit all Data that saved at TxD Buffer

5) ST-5232

- 2 Channel Serial Interface RS-485 Terminal Type

◆ Module View



Mapping Data into the image tab.

◆ I/O Process Image Table

- Input Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Status Byte(1CH)	TPA	IL2	IL1	IL0	OR	RR	TA	IA
Byte#1	Data Byte#0(1CH)								
Byte#2	Data Byte#1(1CH)								
Byte#3	Data Byte#2(1CH)								
Byte#4	Data Byte#3(1CH)								
Byte#5	Data Byte#4(1CH)								
Byte#0	Status Byte(2CH)	TPA	IL2	IL1	IL0	OR	RR	TA	IA
Byte#1	Data Byte#0(2CH)								
Byte#2	Data Byte#1(2CH)								
Byte#3	Data Byte#2(2CH)								
Byte#4	Data Byte#3(2CH)								
Byte#5	Data Byte#4(2CH)								

- Output Data

Byte Offset		Decimal Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte#0	Control Byte(1CH)	TPR	OL2	OL1	OL0	-	RA	TR	IR
Byte#1	Data Byte#0(1CH)								
Byte#2	Data Byte#1(1CH)								
Byte#3	Data Byte#2(1CH)								
Byte#4	Data Byte#3(1CH)								
Byte#5	Data Byte#4(1CH)								
Byte#0	Control Byte(2CH)	TPR	OL2	OL1	OL0	-	RA	TR	IR
Byte#1	Data Byte#0(2CH)								
Byte#2	Data Byte#1(2CH)								
Byte#3	Data Byte#2(2CH)								
Byte#4	Data Byte#3(2CH)								
Byte#5	Data Byte#4(2CH)								

- Status Byte

- IA : Initialization Acknowledge
- TA : Transmit Acknowledge
- RR : Receive Request
- RBO : RxD Buffer Overrun Error
  There are two counters (Run counter and Index Counter) which pointing at the position of RxD Buffer. Run counter is increased +1 whenever RxD input, Index counter is increased as much as Input length that brought on Input data.
  Therefore, if (Run counter - Index counter)>1024(RxD Buffer Size), RxD Buffer Overrun error occurs.
- IL0~IL2 : Input length
- TPA : Transmit Processing Acknowledge
  (Related Configuration Parameter : TxD Buffering)

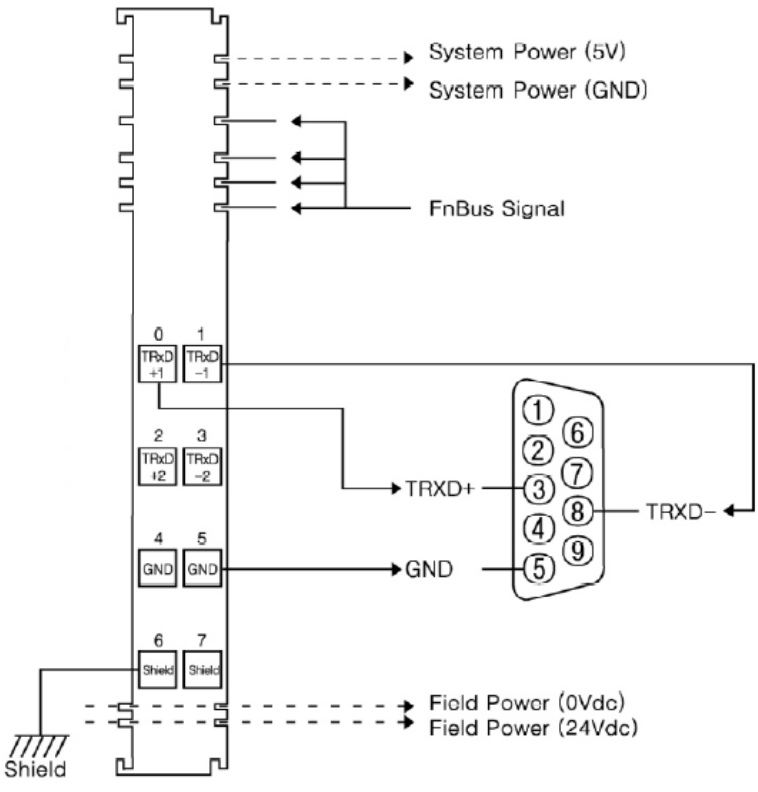
- Control Byte

- IR : Initialization Request
- TR : Transmit Request
- RA : Receive Acknowledge
- OL0~OL2 : Output Length
- TRR : Transmit Processing Request
  (Related Configuration Parameter : TxD Buffering)

◆ Specification

Input Specification	
Transfer Channels	TxD, RxD, Half Duplex
Transfer Rate	300~115200bps
Data Bit	7bit, 8bit, 9bit
Parity Bit	None, Odd, Even
Stop Bit	1bit, 2bit
Bit Distortion	<1.6%
Connection	Spring force of RTB
Cable Length	1㎞ twisted pair
Line Impedance	120ohm
Data Buffer	In/Out User Data 10Bytes, Control/Status 2byte
RxD Buffer	1024bytes
TxD Buffer	256bytes
Input Image Size	12bytes
Output Image Size	12bytes
Module Specification	
Power Dissipation	Max. 155mA @ 5.0Vdc
Isolation	Photo-coupler Isolation, Isolation Voltage : 1000Vrms/Vac
Size	12mm × 99mm × 70mm

◆ Module Wire Diagram



- Wiring Description

Pin No.	Description	Pin No.	Description
0	TRxD +1	1	TRxD -1
2	TRxD +2	3	TRxD -2
4	GND	5	GND
6	Shield	7	Shield

◆ Configuration Parameter Table

Offset	Decimal Bit							
Byte#0	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2it**	**1Bit**	**0it**
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Other : Unused Default : 00		Data Bit 00 : 7Data bit 01 : 8Data bit 10 : 9Data bit Other : Unused Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010 : 2400bps 0011 : 4800bps 0100 : 9600bps (Default Value) 0101 : 19200bps 0110 : 38400bps 0111 : 57600bps 1000 : 115200bps Other : Unused			
Byte#1	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved						TxD Process 0:Disable 1:Enable Default:0 Note 1	Stop BIt 0 : 1bit 1 : 2bit Default : 0
Byte#2	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Other : Unused Default : 00		Data Bit 00 : 7Data bit 01 : 8Data bit 10 : 9Data bit Other : Unused Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010 : 2400bps 0011 : 4800bps 0100 : 9600bps (Default Value) 0101 : 19200bps 0110 : 38400bps 0111 : 57600bps 1000 : 115200bps Other : Unused			
Byte#3	**7Bit**	**6Bit**	**5Bit**	**4Bit**	**3Bit**	**2Bit**	**1Bit**	**0Bit**
	Reserved						TxD Process 0:Disable 1:Enable *Default:0 *Note 1	Stop Bit 0 : 1bit 1 : 2bit Default : 0

*Note 1

Disable : Transmit immediately Output Data #0~ Output Data #4

Enable : Store the value of Output Data continually at RxD Buffer of Serial Interface Module When TPA bit and TPR bit of Control Byte and Status Byte are different, transmit all Data that saved at TxD Buffer

※ **Example**

◆ **Initialization of the Module**

- Control Byte

- Set bit in control byte to '1'.
- Receive and Transmit functions are stopped.
- RxD Buffer and TxD Buffer are erased.
- Serial Interface Module will set configuration parameter value.

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	x	x	x	x	x	x	x	IR

- Status Byte

- If IA in Status Byte set to '1', Initialization of serial interface module success.

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	x	x	x	x	x	x	x	IA

◆ **Example of Transmitting data (Transmit Data "CREVIS.CO.KR")**

- Step #0

- TR inverting (TR ≠ TA)
- Output Length = 5
- Output Data = "CREVI"

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	0	0

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	x	1	0
Output Byte #0	'C' (0x43)							
Output Byte #1	'R' (0x52)							
Output Byte #2	'E' (0x45)							
Output Byte #3	'V' (0x56)							
Output Byte #4	'I' (0x49)							

- Step #1

- Check TA bit value in Status Byte.
- TR = TA : transmit complete.

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	1	0

- Step #2

- TR inverting (TR ≠ TA)
- Output Length = 5
- Output Data = “S.CO.”

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	x	0	0
Output Byte #0	'S' (0x53)							
Output Byte #1	'.' (0x2E)							
Output Byte #2	'C' (0x43)							
Output Byte #3	'O' (0x4F)							
Output Byte #4	'.' (0x2E)							

- Step #3

- Check TA bit value in Status Byte.
- TR = TA : transmit complete.

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	0	0

- Step #4

- TR inverting (TR ≠ TA)
- Output Length = 1
- Output Data = “KR”

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	0	0	1	x	x	1	0
Output Byte #0	'K' (0x4B)							
Output Byte #1	'R' (0x52)							
Output Byte #2								
Output Byte #3								
Output Byte #4								

- Step#5

- Check TA bit value in Status Byte.
- TR = TA : transmit complete.

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	1	0

◆ Example of Receiving data (Receive Data "Welcome")

- Step #0
- RR = RA

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	0	x	0

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	0	x	0

- Step #1

- RA inverting (RA ≠ RR)

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	1	x	0

- Step #2

- RR inverting (RA = RR)
- Input Length = 5
- Input Data = "Welco"

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	1	x	0
Input Byte #0	'W' (0x57)							
Input Byte #1	'e" (0x65)							
Input Byte #2	'l' (0x6C)							
Input Byte #3	'c' (0x63)							
Input Byte #4	'o' (0x6F)							

- Step #3

- RA inverting (RA ≠ RR)

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	0	x	0

- Step #4

- RR inverting (RA = RR)
- Input Length = 2
- Input Data = “me”

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	0	1	0	x	0	x	0
Input Byte #0	'm' (0x57)							
Input Byte #1	'e' (0x65)							
Input Byte #2	0x00							
Input Byte #3	0x00							
Input Byte #4	0x00							

◆ TPR and TPA Example (“Welcome ”)

- Step #0

- TxD Process data in Configuration Parameter set to “1” (Enable).

- Step #1

- TR inverting (TR ≠TA)
- Output Length = 5
- Output Data = “Welco”

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	0	x	x	x	x	x	0	0

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	0	1	0	1	x	x	1	0
Output Byte #0	'W' (0x57)							
Output Byte #1	'e" (0x65)							
Output Byte #2	'l' (0x6C)							
Output Byte #3	'c' (0x63)							
Output Byte #4	'o' (0x6F)							

- Step #2

- Check TA bit value in Status Byte.
- TR = TA : transmit complete.

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	0	x	x	x	x	x	1	0

- TxD Buffer

Offset	TxD Buffer Data
0	'W' (0x57)
1	'e" (0x65)
2	'l' (0x6C)
3	'c' (0x63)
4	'o' (0x6F)
5	
6	
7	
⋮	⋮
254	
255	

- Step #3

- TR inverting (TR ≠TA)
- Output Length = 2
- Output Data = “me”

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	0	0	1	0	x	x	0	0
Input Byte #0	'm' (0x57)							
Input Byte #1	'e' (0x65)							
Input Byte #2	0x00							
Input Byte #3	0x00							
Input Byte #4	0x00							

- Step #4

- Check TA bit value in Status Byte.
- TR = TA : transmit complete.

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	0	x	x	x	x	x	0	0

- TxD Buffer

Offset	TxD Buffer Data
0	'W' (0x57)
1	'e' (0x65)
2	'l' (0x6C)
3	'c' (0x63)
4	'o' (0x6F)
5	'm' (0x57)
6	'e' (0x65)
7	
⋮	⋮
254	
255	

- Step #5

- TPR inverting (TPR ≠ TPA)

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	1	0	1	0	x	x	0	0

- Transmit all TxD Buffer data. (TxD Buffer empty)

Offset	TxD Buffer Data
0	
1	
2	
3	
4	
5	
6	
7	
⋮	⋮
254	
255	

- Step #6

- Check TPA bit value in Status Byte.
- TPR = TPA : transmit complete.

	7 bit	6 bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	1	x	x	x	x	x	0	0

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